The present invention also relates to a data processing installation having at least one processor, a bootstrap memory unit, a reload memory unit and having a main memory unit. The bootstrap memory unit and/or the reload memory unit is a memory unit with serial data access or a memory unit which requires a number of read operations in order to read a program command. In developments, the data processing installation is designed such that, when it is operating, the inventive process or one of its developments is performed. Hence, the technical effects mentioned above also apply to the data processing installation.

The present invention also relates to a circuit arrangement, e.g. a user-specific circuit (ASIC), which is required as a control unit when performing a start operation including a serial memory unit. In one embodiment, the circuit arrangement is designed such that, when it is operating, the inventive process or one of its developments is performed. The technical effects mentioned above also apply to the circuit arrangement.

The present invention also relates to the use of a serial-access memory unit as a memory for program data in a start operation for a data processing installation. In particular, multimedia cards and the other cards mentioned above and the Memory Stick memory unit have to date been used only for storing music data or voice data, but not for storing program data. The technical effects mentioned above also apply to the use of the serial memory unit.

Additional features and advantages of the present invention are described in, and will be apparent from, the following Detailed Description of the Invention and the Figures.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 shows circuit units required for the start operation in a data processing installation.

Figure 2 shows a flowchart containing process steps for restarting the data processing installation.

Figure 3 shows memory areas in a reload memory.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows circuit units used for the start operation in a data processing installation 10. These circuit units include a processor 12, a main memory 14, a bootstrap memory 16, a reload memory 18 and an ASIC 20. The processor 12 is a microcontroller, e.g. of the "Coldfire" type, as manufactured by MOTOROLA. A bus system 22 connects the processor 12 to the ASIC 20. The bus system 22 contains, like the processor 12, thirty-two data lines, a number of control lines and a multiplicity of address lines.

The main memory 14 is a commercially available SDRAM (Synchronous Dynamical Random Access Memory). A bus system 24 connects the main memory 14 to the ASIC 20. The bus system 24 contains a number of data lines, e.g. sixteen data lines, a number of control lines and a multiplicity of address lines. The main memory 14 has a storage capacity of 32 megabytes, for example.

The bootstrap memory 16 is a serial EEPROM having a storage capacity of, by way of example, 32 kilobytes; for example, an EEPROM from PHILIPS with an IIC bus system. The bootstrap memory 16 contains a bootstrap program. A bus system 26 connects the bootstrap memory 16 to the ASIC 20. The bus system 26 contains just one control line and a line for data transfer.

The reload memory 18 contains a multimedia card having a storage capacity of 16 megabytes, for example. By way of example, a multimedia card from SCANDISC is used. The reload memory 18 stores the operating system; e.g., the WINDOWS operating system. The reload memory 18 is connected to the ASIC 20 via a serial interface 28 containing seven lines, one line of which is used for transferring the data.

The ASIC 20 contains a processor interface unit 30 for connecting the bus system 22, a controller unit 32 for connecting the bus system 24, a bootstrap memory interface unit 34 for connecting the IIC bus, and a reload memory interface unit 36 for connecting the serial interface 28. The ASIC 20 also contains a control unit 38. The interface units 30, 34 and 36, the controller unit 32 and the control unit 38 are connected inside the ASIC 20 via an internal bus system 40.

The processor interface 30 forms the interface between the bus system 22 and the internal bus system 40. The internal bus system essentially corresponds to the bus system 22, wherein only small signal adjustments need to be made in the interface unit 30.

The controller unit 32 forms the interface between the bus system 24 and the internal bus system. In addition, the controller unit 32 is used for synchronizing the read and write access operations on the main memory 14.

The bootstrap memory interface 34 connects the IIC bus system 26 to the internal bus system 40. The interface unit 34 contains a serial/parallel data converter, which produces data words from the bits coming from the bootstrap memory 16 and forwards them to the internal bus system 40. The interface unit 34 also contains a register for storing data words transferred via the internal bus system 40. On the basis of the content of these data words, control signals for controlling the read operation of the bootstrap memory 16 are produced on the control line of the bus system 26.

The interface unit 36 connects the serial interface 28 to the internal bus system. The interface unit 36 contains a serial/parallel data converter which is used to convert data arriving via the interface 28 into data words having a prescribed number of bit positions; e.g., having 32 bit positions.

The control unit 38 contains a start controller 42 and a bus access circuit 44. The start controller 42 is connected to a reset line 46. If a reset signal is produced on the reset line 46, the start controller 42 starts to control a start operation, which is explained in more detail below with reference to Figure 2. The bus access circuit 44 ensures that there are no conflicts during access by the units connected to the internal bus system 40.

Figure 2 shows a flowchart containing process steps which are performed when the data processing installation 10 is restarted; see also Figure 1. The process starts in a process step 100 with the production of a reset pulse on the reset line 46.

In a subsequent process step 102, the start controller 42 uses the bootstrap memory interface unit 34 to copy the bootstrap program's program commands